second control structures **400** extending through the barrier zone **125** into the drift zone **121**. One, two, three or more field electrode structures **170** may be formed between each control structure **420** assigned to the auxiliary cells AC and gate structures **150** assigned to the transistor cells TC. The field electrode structures **170**, the gate structures **150** as well as the second control structures **400** may have the same vertical extension and/or the same lateral cross-sectional area. The cross-sectional areas of each of the second control structures **400**, gate structures **150** and field electrode structures **170** may be polygons, for example squares or rectangles with or without rounded corners, ovals, circles or rings. According to other embodiments, the control structures **400**, the field electrode structures **170** and the gate structures **150** are stripe-shaped and form a regular stripe pattern.

First portions of the control electrode **420** included in the gate structures **150** and second portions of the control electrode **420** in the second control structures **400** are electrically coupled or connected to the gate terminal G. Field dielectrics **171** electrically separate a field electrode **175** from the semiconductor body **100**. The field electrodes **175** may float or may be electrically connected to the potential of one of the load electrodes. For example, the field electrodes **175** may be electrically connected to the emitter terminal E.

The IGFET **540** of FIG. **9**B is also based on the concept of the semiconductor switching device **500** of FIG. **7**A. The charged layer **415** is formed along the sidewalls of the control structure **400** and is absent in a bottom portion to reduce gate-to-collector capacitance C_{GD}. A contact layer **129** of the first conductivity type is effective as a drain layer. The first load terminal provides a source terminal S and the second load terminal provides a drain terminal D. As regards further details, reference is made to the description of FIG. **9**A.

According to the embodiment illustrated in FIG. **10**A, second control structures **400** and gate structures **150** alternate with each other, wherein at least one, for example two, three or more, field electrode structure **170** are arranged between neighboring second control and gate structures **400**, **150**.

The semiconductor device **510** of FIG. **10**B is based on a layout without field electrode structures. First semiconductor mesas **160***a* with source zones **110** alternate with second semiconductor mesas **160***b* without source zones **110**. Charged layers **415** are only formed along the second semiconductor mesas **160***b*. Second control structures **400** face each other at opposing sides of an intermediate second semiconductor mesa **160***b*. Gate structures **150** face each other on opposing sides of intermediate first semiconductor mesas **160***a*. Second control structures **400** and gate structures **150** share the same main trenches.

FIG. **10**C refers to an embodiment with all charged layers **415** formed on the same side of main trench structures. For example, after forming the main trench structures and the control dielectrics, silicon and/or germanium atoms may be implanted at an implant angle tilted to the perpendicular such that the intermediate semiconductor mesas **160** shadow the implant beam. The source zones **110** are formed only in the halves of the semiconductor mesas **160** averted from the control structure **400** and facing the respective gate structure.

FIG. **11** refers to an embodiment with planar second control and gate structures **400**, **150**. The lateral extension of the charge carrier transfer zones **118** may be smaller than that of the body zones **115** such that the second control structures **400** overlap with portions of the drift zone **121**.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that a variety of alternate and/or equivalent implementations may be substituted for the specific embodiments shown and described without departing from the scope of the present invention. This application is intended to cover any adaptations or variations of the specific embodiments discussed herein. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A semiconductor device, comprising:

a first load terminal electrically connected to source zones of transistor cells, wherein the source zones form first pn junctions with body zones;

a second load terminal electrically connected to a drain construction forming second pn junctions with the body zones; and

control structures directly adjoining the body zones, the control structures comprising a control electrode and charge storage structures, the control electrode configured to control a load current through the body zones, the charge storage structures insulating the control electrode from the body zones and containing a control charge adapted to induce inversion channels in the body zones in the absence of a potential difference between the control electrode and the first load terminal,

wherein the body zones are formed in semiconductor mesas formed from portions of a semiconductor body and separated from each other by the control structures.

2. The semiconductor device of claim **1**, wherein the charge storage structures are sandwiched between the control electrode and at least the body zones.

3. The semiconductor device of claim **1**, wherein the charge storage structures are charged portions of a control dielectric that separates the control electrode from a semiconductor body including the body zones.

4. The semiconductor device of claim **1**, wherein the charge storage structures comprise charge storage layers, first dielectrics sandwiched between the body zones and the charge storage layers, and second dielectrics sandwiched between the charge storage layers and the control electrode.

5. The semiconductor device of claim **4**, wherein the charge storage layers comprise a conductive material.

6. The semiconductor device of claim **5**, further comprising:

a wiring structure connecting the charge storage layers with a programming pad.

7. The semiconductor device of claim **4**, wherein the charge storage layers comprise dielectric charge trapping layers.

8. The semiconductor device of claim **4**, wherein the first dielectric is thicker than the second dielectric.

9. The semiconductor device of claim **4**, further comprising:

program electrodes sandwiched between the control electrode and the charge storage layers.

10. The semiconductor switching device of claim **1**, wherein the charged layer is a dielectric structure embedding semiconducting nanocrystallites.

11. A semiconductor switching device, comprising:

transistor cells comprising source zones forming first pn junctions with body zones, the body zones forming second pn junctions with a drain construction;